A 450MHz CMOS RF Power Detector

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Abstract **- A RF Power Detector based on a CMOS logarithmic/limiting amplifier achieves 50dB dynamic range at 450MHz. The logarithmic accuracy is +/- 1dB over the temperature range 0 to 85 degC. The chip is fabricated in 0.35um double-poly triple-metal CMOS and consumes 10mA with a 3V supply.**

I. Introduction

One method for RF power control in a mobile communications handset is to use a power detector to measure the RF power at the antenna during transmit and produce a voltage that corresponds to the log of the power. The power detector is incorporated within a control loop as shown in Figure 1 to control the PA output power within specified limits. Since the power detector determines the accuracy of the output power level, it must have a linear transfer function which is stable over temperature. This paper presents a RF power detector fabricated in 0.35um CMOS which achieves 50dB dynamic range at 450MHz with +/- 1dB accuracy over the temperature range 0 to 85 degC. The detector also achieves log conformance out to 900MHz, making it potentially suitable for GSM applications.

II. Architecture

The RF power detector is a based on a successive detection CMOS logarithmic amplifier ("log-amp"). CMOS was chosen for both low cost and high levels of integration. Previously reported CMOS log-amps [1]-[3] have used this method at low IF frequencies (100-450kHz) for RSSI and as a limiting amplifier in IF strips. In contrast, a Si bipolar log-amp [4] using the successive detection method achieved 60dB dynamic range at 2GHz, but consumes 250mW on a 3V supply. Recent commercially available log-amps [5] consume considerably less power.

A block diagram of the successive detection log-amp is shown in Figure 2. It consists of a cascade ("log-strip") of 6 CMOS limit amplifiers which have a gain of 9dB in their linear region and limit above a certain input level. The DC transfer function of the log-strip is

$$V_{out} = V_{slope} * \log_{10}(V_{in}/V_{intercept})$$

With the input terminated by a 50Ω resistor, the transfer function can be expressed in terms of input power. In this case, the units for V_{slope} and $V_{intercept}$ are volts/dB and dBm, respectively.

As shown in Figure 2, a rectifying transconductor cell is placed at the input port and at the output of each of the limit amplifiers. The outputs of the rectifying transconductors are summed together and low pass filtered to produce a voltage proportional to the log of the input. For constant envelope RF inputs (such as in GSM), the output voltage is actually a measure of the amplitude of the carrier envelope, and not of true RMS power.

III. Circuits

The dynamic range of the log-strip is determined by the number of stages in the cascade and the gain of each stage. For operation between 450MHz and 1900MHz (corresponding to the GSM bands in use), the limit amplifiers must have a flat frequency response up to 2GHz in order to service all bands. Furthermore, the response must be stable over temperature. Figure 3 shows the circuit used to achieve this. The limit amplifier is a resistively loaded NMOS differential pair with an NMOS cascode with a bit of positive feedback. The positive feedback has two functions: it bootstraps the drains of the input devices to their gates, thus eliminating the Miller effect, and it gives a gain boost by appearing as a negative resistance. This method for widebanding the simple resistively loaded differential pair is based on a bipolar technique. Source followers are used to level shift the output down to drive the next stage and to decouple the load resistance from the input capacitance of the next stage.

The gain of the limit amplifier is set by g_m*R_{load}. In order to stabilize the gain over temperature, a constant-g_m replica bias is used [6]. The circuit, shown in Figure 3, is set up to make g_m of the input differential pair proportional to the inverse of a resistance. The resistance is of the same type as the load resistor in the limit amplifier, thus setting the gain equal to the ratio of two like resistors. Two diode-connected NMOS devices, MN1 and MN2, impress a ΔV_{gs} across resistor R1. The loop forces nodes A and B to be the same, as well as currents I1 and I2. As a result, the body effect for devices MN1 and MN2 is the same and their Vt's will be equal to first order. ΔV_{gs} is then a function of device geometry alone and g_m is equal to

$$g_{m1} = 2 * [1\text{-sqrt}(W/L_1/W/L_2)]/R_1$$

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This relationship is not exact because of the output impedances of MN1 and MN2. As a result, g_{m1} contains a slight negative TC. This has been compensated for by using a POLY1 type resistor in the bias cell, which has a lower positive TC than the POLY2 type resistor used in the limit amplifiers.

The rectifying transconductor is shown in Figure 4. In order to achieve rectification of the input signal, it uses two unbalanced source-coupled pairs [3]. The difference in the device widths creates a positive offset in one of the source coupled pairs such that one side is completely turned off in the presence of zero input signal. The input is reversed and applied to a second source-coupled pair which creates a negative offset. The outputs of each of the source-coupled pairs which are shut off with zero input signal are summed together to produce the rectified output. A mismatch in the two pairs will cause the rectified output to become unsymmetric around zero input. While this causes an offset in the full scale output current, it has no effect on the dynamic range of the log-amp. The bandwidth of the rectifying transconductor need not be as high as that of the limit amplifiers. If the transconductor gain rolls off with frequency, the full scale output current will be decreased, but the dynamic range of the log-amp is unchanged.

DC coupling of the limit amplifiers requires an offset compensation loop, otherwise offsets will saturate the signal chain. As shown in Figure 2, an offset feedback loop from the last stage to the first is used. The output from the final limit amplifier is low-pass filtered by an on-chip100k resistor and 50pF capacitor and fed into a weak transconductance stage that drives the input of the first limit amplifier. This offset compensation technique continues to work even when several or all of the limit amplifiers are limiting.

The calculated noise of the log-strip is based on a few assumptions. Since the cascade of limit amplifiers is compressive, i.e. the overall gain decreases as signal level increases, the total output noise is highest at lowest signal level. In addition, it is assumed that the noise in the cascade dominates the noise in the rectifying transconductors since each of the transconductors is preceded by the gain of the cascade in front of it (except for the first one). Based on these assumptions, the input-referred noise of the log-strip is found when all the limit amplifiers are in their linear region. Simulation shows this noise is 180uVrms, well below the threshold of the log-amp. The lower threshold of -50dBm (referred to 50Ω) corresponds to 700uVrms.

IV. Measured Results

As shown in Figure 2, the rectifying transconductor outputs are summed into an on-chip 1st-order low-pass filter. This amplifier can be reconfigured as an integrator to implement a complete power control loop. The measured performance of the power detector is summarized in Table 1 for a 450MHz input. The input range over which the power detector achieves less than +/- 1dB of error over the temperature range 0 to 85 degC is -45dBm to +5dBm. Figure 5 shows the measured transfer characteristic and error. The nominal slope is -7mV/dB. Note that the intercept point varies with temperature. This is an expected result due to the successive detection architecture and can be compensated for by introducing a PTAT correction current to the summing node of the low-pass filter. Figure 5 also shows the performance at 900MHz. Despite a clear degradation in sensitivity, the slope indicates the limit amplifier is maintaining constant gain out to 900MHz. This demonstrates the feasibility of using 0.35um CMOS for GSM and the potential for extending the frequency range out to 2GHz by migrating to a finer geometry process.

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Table 1: Measured Results

Frequency	450MHz
Dynamic Range	50dB
Dynamic Range at 900MHz	25dB
Input range	-45dBm to +5dBm
Error	+/- 1dB
Supply Voltage	3V
Supply Current	10mA
Area	0.5mm^2
Technology	0.35µm double-poly triple-metal CMOS

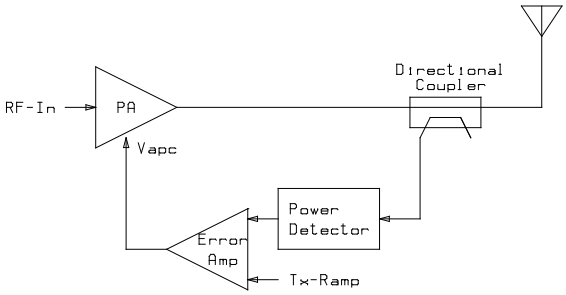


Figure 1: Power Control Loop

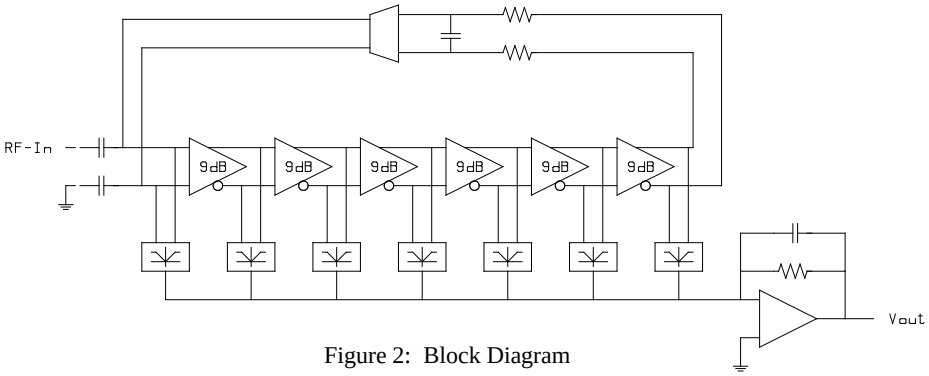


Figure 2: Block Diagram

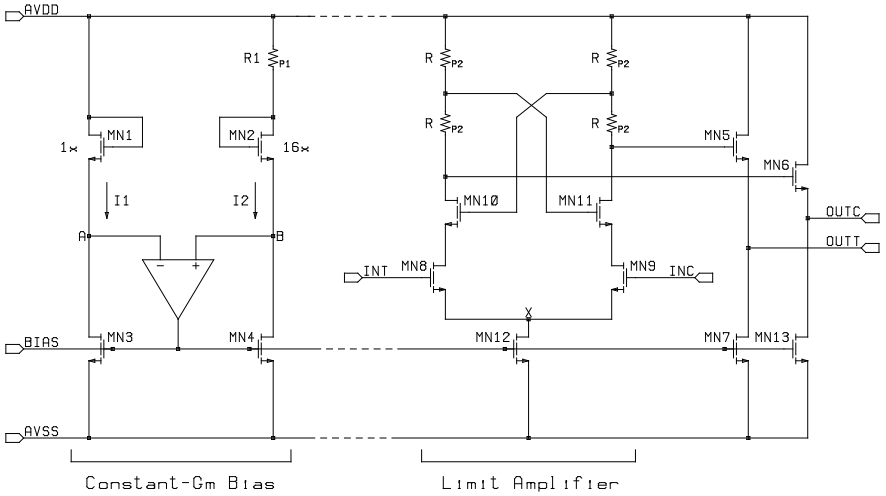


Figure 3: Limiting Amplifier and Bias

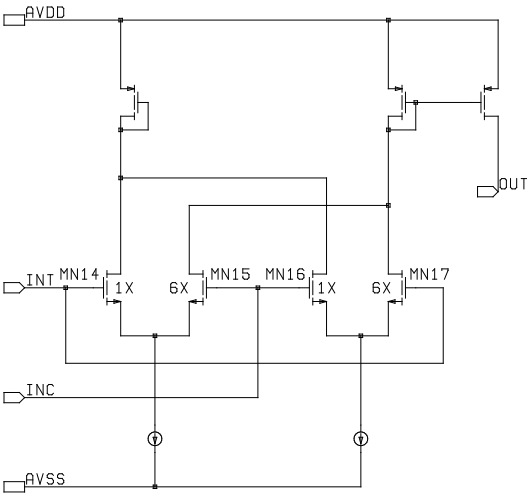
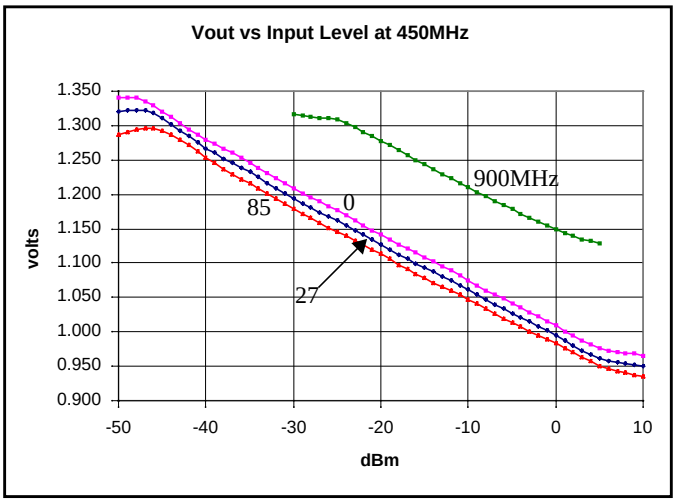
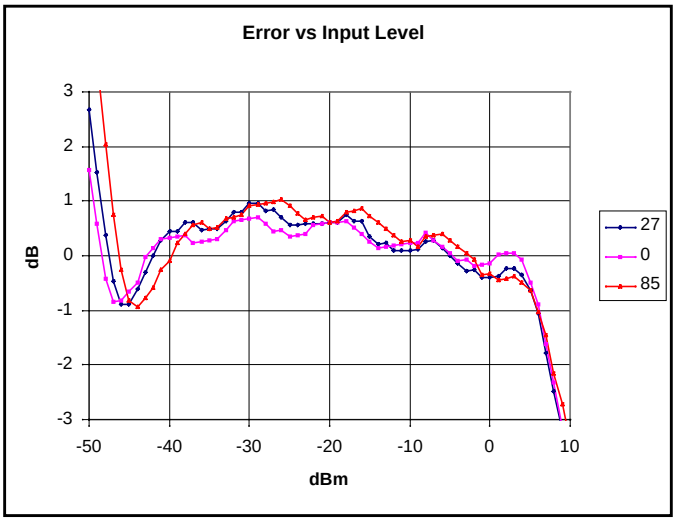


Figure 4: Rectifying Transconductor



(a)



(b)

Figure 5: (a) Measured Transfer Characteristic (b) Error